

Appl. No. 10/749,910
Amdt. dated August 22, 2006
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2181

PATENT

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory controller, comprising:
at least one bus interface, each bus interface being for connection to at least one
respective device for receiving memory access requests;
a memory interface, for connection to a memory device over a memory bus;
a plurality of buffers in the memory interface; and
control logic, for placing received memory access requests into a queue of
memory access requests,
wherein, in response to a received memory access request requiring multiple data
bursts over the memory bus, data from each of said multiple data bursts is assigned by the
control logic to a respective buffer of the plurality buffers in the memory interface, and data from
each of said multiple data bursts is stored by the memory interface in [[a]] the respective buffer,
and of said plurality of buffers, and
wherein, for a wrapping memory access request requiring multiple buffers, data
required for a beginning and an end of the wrapping memory access request are ~~stored in~~
assigned to a single respective buffer of the plurality of buffers by the control logic and stored in
the single respective buffer by the memory interface.
2. (Previously Presented) A memory controller as claimed in claim 1,
wherein, when returning data to the respective device from which a memory access request
requiring multiple data bursts over the memory bus was received, data is read out from a first
part of the single buffer, then data is read out from at least one other of said buffers, then data is
read out from a second part of the single buffer.

Claims 3-4. (Canceled)

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5. (Original) A memory controller as claimed in claim 1, wherein the control logic determines whether a received read access request is a wrapping request which requires multiple memory bursts, and, if so, the control logic allocates each of said memory bursts to a respective one of said buffers.

6. (Original) A memory controller as claimed in claim 1, wherein the memory controller is a SDRAM controller, and said memory interface is suitable for connection to a SDRAM memory device over said memory bus.

7. (Currently Amended) In a memory controller, ~~comprising:~~ including at least one bus interface, ~~each bus interface being for connection to at least one respective device for receiving memory access requests, [[:]] a memory interface [[:]] for connection to a memory device over a memory bus, [[:]] a plurality of buffers in the memory interface, [[:]] and control logic [[:]] for placing received memory access requests into a queue of memory access requests, a method of retrieving data comprising:~~

~~in response to a received memory access request requiring multiple data bursts over the memory bus, assigning each data burst to a respective buffer in a plurality of buffers in the memory interface; and~~

~~storing data from each of said multiple data bursts in [[:a]] the respective buffer in the memory interface, of said plurality of buffers;~~

~~wherein, for a wrapping memory access request, data required for a beginning and an end of the wrapping memory access request are assigned to a single respective buffer by the control logic and stored in [[:a]] the single respective buffer of the plurality of buffers in the memory interface.~~

8. (Previously Presented) A method as claimed in claim 7, further comprising, when returning data to the respective device from which a memory access request requiring multiple data bursts over the memory bus was received, reading data out from a first

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part of single buffer, then reading data out from at least one other of said buffers, then reading data out from a second part of the single buffer.

Claims 9 - 10. (Canceled)

11. (Currently Amended) A method as claimed in claim 7, further comprising determining whether a received read access request is a wrapping request which requires multiple memory bursts, and, if so, allocating performing the step of assigning each of said memory data bursts to a respective one of said buffers.

12. (Original) A method as claimed in claim 7, wherein the memory controller is a SDRAM controller, and said memory interface receives data from a SDRAM memory device over said memory bus in SDRAM bursts.

13. (Currently Amended) A programmable logic device, wherein the programmable logic device includes a memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective device formed within the programmable logic device for receiving memory access requests;

a memory interface, for connection to an external memory device over a memory bus;

a plurality of buffers in the memory interface; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, ~~data from~~ each of said multiple data bursts is assigned by the control logic to a respective buffer of the plurality buffers in the memory interface, and data from each of said multiple data bursts is stored by the memory interface in [[a]] the respective buffer, and of said plurality of buffers, and

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wherein, for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are ~~stored in assigned to a single respective buffer of the plurality of buffers by the control logic and stored in the single respective buffer by the memory interface.~~

14. (Currently Amended) A memory controller as recited in claim 1, wherein each of the plurality of buffers is a sub-buffer of a larger memory buffer in the memory interface. ~~includes a plurality of sub-buffers, data required for the beginning and the end of the wrapping memory access request being stored in separate sub-buffers of the single buffer.~~

15. (Currently Amended) A memory controller as recited in claim ~~[[14]]~~ 1, wherein the control logic is operable to record the value of a pointer indicating the sub-buffer single respective buffer from which data required for the end of the wrapping memory is to be retrieved, ~~from the single buffer.~~

16. (Currently Amended) A method as recited in claim 7, wherein each of the plurality of buffers is a sub-buffer of a larger memory buffer in the memory interface. ~~includes a plurality of sub-buffers, data required for the beginning and the end of the wrapping memory access request being stored in separate sub-buffers of the single buffer.~~

17. (Currently Amended) A method as recited in claim ~~[[16]]~~ 7, wherein the control logic is operable to record the value of a pointer indicating the sub-buffer single respective buffer from which data required for the end of the wrapping memory is to be retrieved, ~~from the single buffer.~~